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PATENT ABSTRACTS OF JAPAN(21) Application number: **03164830**(51) Intl. Cl.: **H01L 21/66 G01R 31/28 H01L 27/04**(22) Application date: **05.07.91**

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publication: **22.01.93**(84) Designated contracting
states:(71) Applicant: **NEC KYUSHU LTD**(72) Inventor: **NAKAJIMA TOSHIHIKO**

(74) Representative:

**(54) SEMICONDUCTOR
INTEGRATED CIRCUIT**

(57) Abstract:

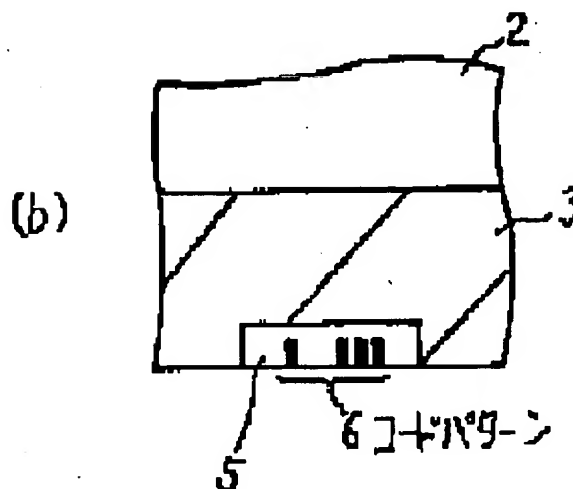
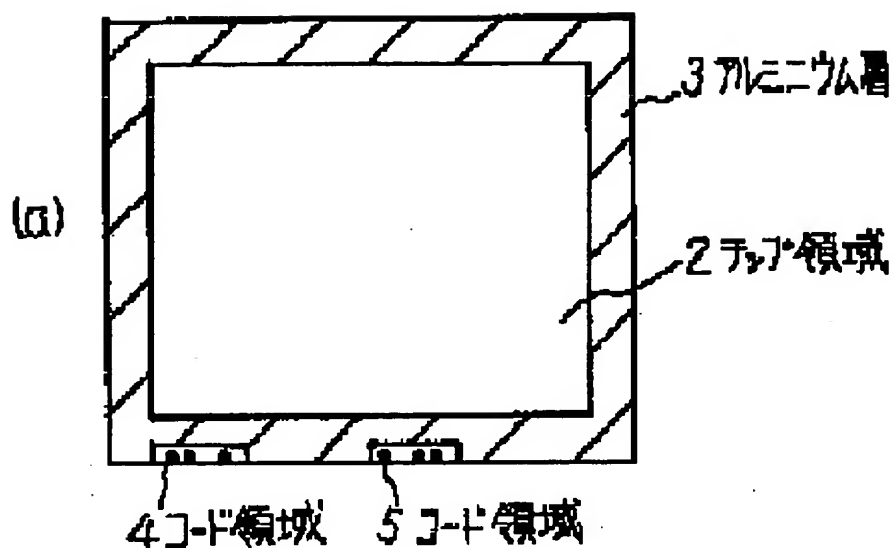
PURPOSE: To improve manufacturing efficiency at the time of manufacturing by incorporating an identification code into each piece of semiconductor integrated circuit at the time of a stepper exposure of a patterning process of an aluminum layer.

CONSTITUTION: An aluminum layer 3 is provided around a chip area 2 provided on a semiconductor wafer, and when the aluminum layer 3 is processed by patterning, a code pattern 6 which is made by patterning individual identification code corresponding to respective chips is formed within code areas 4 and 5 by a stepper exposure. The information of each chip is optically read at the time of electrical characteristic test of a semiconductor integrated circuit on the chip, and its judging results on good or bad, grade information, etc., can be recorded on a memory cell

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provided on the respective chips, so that only the chips of intended grade can be selected for fabrication, resulting in eliminating a products stock which are not required.

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